Debugging Digital Signals

Practical Tips & Techniques

As speeds increase and designs shrink, timing errors and physical layer issues create signal integrity problems in today's digital designs. These problems can become incorrect data patterns unless properly addressed. With the right oscilloscope and the tips outlined here, you can analyze your digital design and its signals faster than ever before to find and troubleshoot signal integrity problems.

Timing Errors

Timing errors may result in incorrect binary values on a bus.

Bus Contention

Symptom: Runt, glitch

Occurs when two drivers try to use the same bus line at the same time. Normally, one of the drivers should go to a high impedance state and not hinder the other while it sends data. If the high impedance device doesn't change in time, the two drivers then contend for the bus. Neither driver prevails, forcing the bus to an indeterminate amplitude that may fail to reach the threshold voltage.

Metastability

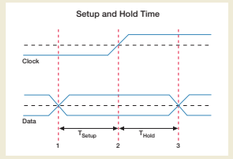
Symptom: Runt, glitch, wrong logic level

An indeterminate or unstable data state that results from a timing violation. As a result, the output signal might be late or achieve an illegal output level, such as a runt, a glitch, or even the wrong logic level.

Setup and Hold Violations

Symptom: Glitch, no transition

A clocked device requires the data to be stable at its input for a specified time before the clock arrives. This is known as "setup" time. Similarly, the input data must remain valid for a specified time after the leading edge of the clock. This is known as "hold" time. Violating setup and/or hold requirements can cause unpredictable glitches on the output, or can cause there to be no output transition at all.



Physical Layer Issues

Physical layer issues are usually most evident when looking at the analog characteristics of the signal; these issues can create timing errors or result in digital faults. For instance, when low-amplitude signals turn into incorrect logic states, or when slow rise times cause pulses to shift in time. These phenomena often have their origins in circuit board design or signal termination.

Ground Bounce

Symptom: Runt, glitch, false transition

Ground bounce is a shift in a device's ground reference caused by a current spike in its ground plane. When multiple outputs on a device switch synchronously, they can generate large transient ground currents. The voltage drop across the bond-wire, ground-lead and the return path cause the ground potential inside the device to "bounce" above system ground.

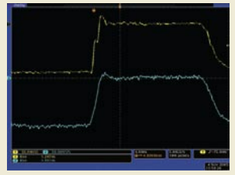
Reflections

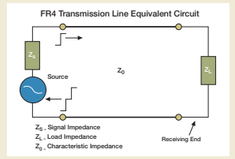
Symptom: Glitch, Setup and hold violation, disruption in transition

Result from mismatched or unterminated lines, causing glitches or other disruptions in the signal transition. Treat a connection like a transmission line when the propagation of the signal down the line and back is longer than it takes to complete the transition (2Tprop > Trise).

Example: For a typical circuit board of FR4 material, the propagation speed is roughly 15 cm/ns. With a 1 ns rise time, any trace longer than 7 cm can have transmission line effects.

The source and destination (receiving end) signals are often different because of reflections and ringing. It is important to probe the receiving end of the line.

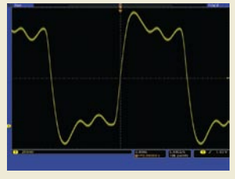




Ringing

Symptom: Ringing, overshoot

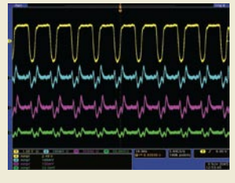
An under damped resonant circuit can cause ringing and overshoot. Inadequate power supply bypassing and attaching long power and ground leads to the device can create this problem. Caution: Poor probing techniques can also introduce ringing and overshoot.



Crosstalk

Symptom: Glitch, setup and hold violation, false transition

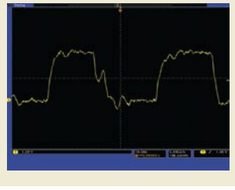
Occurs when asynchronous lines couple into clock lines. Crosstalk causes false transitions or "pulls" clock edges producing timing errors or setup and hold violations. The problem worsens as rise times get faster. Caution: Long probe ground-leads during test can create "false" crosstalk, because long leads can create large circuit-loops.



Amplitude Problems and Edge Aberrations

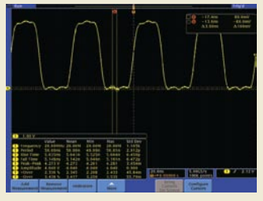
Symptom: Runt, slow rise time, ringing, droop, rounding, overshoot

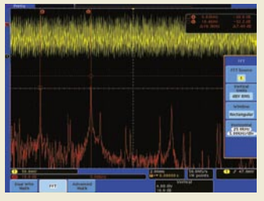
Problems with the analog characteristics of a digital signal. Often a result of board layout problems, improper termination or even quality problems in the semiconductor devices within the design.



Tips & Techniques for Debug

- Check for symptoms of common signal integrity problems by setting up an appropriate trigger. The oscilloscope will then continuously check your signal looking for a pulse that violates the parameters you set. If the oscilloscope triggers, then you know that you have an anomaly in your signal.
- Set up the oscilloscope to monitor your signal for long durations of time – throughout the night or over the weekend – to check the stability of your design. Simply set up an appropriate trigger; the oscilloscope will continue to monitor your signal until the trigger event occurs.
- Quickly find all instances of your trigger event in your waveform, by using an oscilloscope with automated search. This enables you to determine frequency of occurrence.
- Accurately and repeatedly analyze any identified digital faults to determine root cause with built-in waveform analysis tools such as automated measurements and measurement statistics.
- Identify sources of noise in a circuit with the oscilloscope's Fast Fourier Transform (FFT) function. The FFT of your signal will show the component frequencies that make up the signal. With this information, you can then associate those frequencies with known system frequencies, such as system clocks, switching power supplies, etc.
- Verify that the right data is being sent on your bus by using an oscilloscope with automated decode, trigger and search for serial and parallel buses. With these analysis tools, you can quickly verify the data integrity of your bus.





Digital Debug Checklist

- Check digital signals for common symptoms of signal integrity problems:
  - Runts
  - Glitches
  - Slow rise time
  - Setup and hold violations
- Analyze signals for:
  - Overshoot, Undershoot
  - Droop
  - Non monotonic edges
  - Amplitude problems
  - Pulse width
  - Noise
- Verify data integrity on communication buses

Probing Considerations

Probes and probing techniques affect the quality of a measurement. High capacitive loading can slow down signal edges. Inductance from the probe ground-lead combined with capacitance from the probe input form a series-resonant circuit that can appear as ringing.

Tip: Shortening the probe's ground lead and lowering the input capacitance will raise the resonant frequency above the oscilloscope bandwidth. Loading capacitance for conventional probes may be as high as 10 – 15 pF. The right active probe, however, will have < 1 pF of input loading capacitance. This capacitive difference keeps the ringing down and allows the use of longer ground leads.

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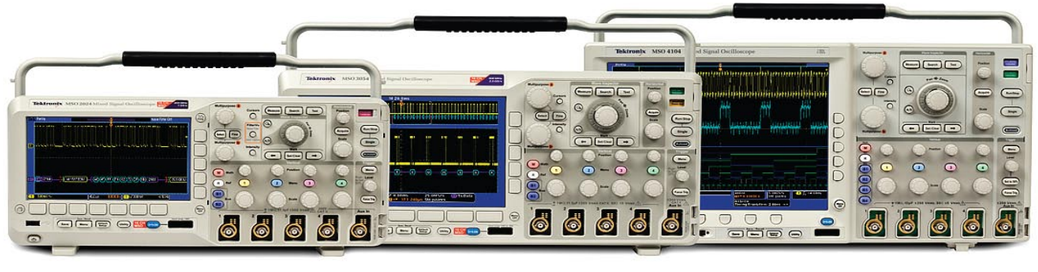

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